ON-CHIP ADVANCED CONTROL ALGORITHM FOR MEMRISTOR OPERATIONS WITH INTEGRATED RISC-V CORE

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KEY RESULTS

- Developed a control algorithm using a RISC-V core to manage a 2×2 memristor array with precision.
- Enabled both voltage and current control modes for the analog conductance control.
- Improved memory performance through dynamic configuration of pulse parameters.
- Validated the accuracy and reliability of control signals using a Universal Verification Methodology Framework (UVMF) testbench.
- Demonstrated the potential of RISC-V and memristor integration for scalable memory systems and neuromorphic computing applications.

INTRODUCTION

As Moore's law encounters fundamental physical limitations, alternative computational approaches, such as neuromorphic computing using elementary memristors, are gaining traction in the scientific community due to several distinct advantages:

- Scalability
- Compatibility with CMOS Technology

Key Challenges:

- **CMOS-Based Control Circuitry:** Managing analog conductance in memristors requires further research in control systems

Project Focus:

- **Flexible Control Architecture:**
  - Utilizing a RISC-V core for adaptable control
  - Designed for both voltage and current control modes in a 2×2 memristor array

Objectives:

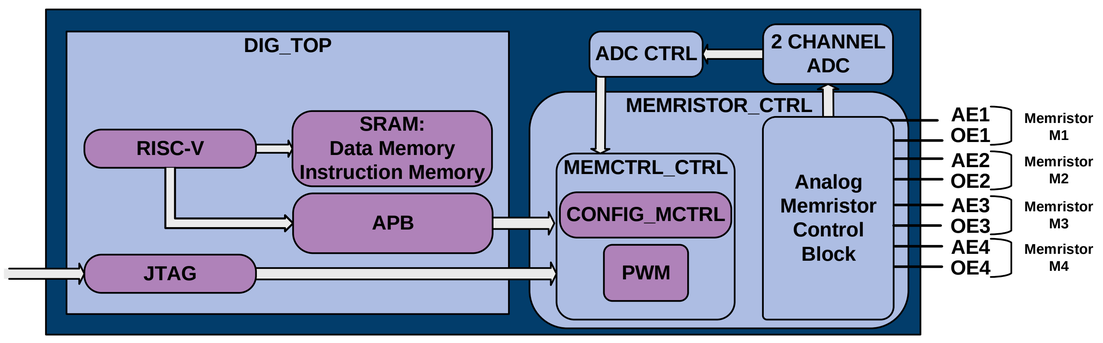
- Develop a flexible control based on Soc

DISCUSSION AND FUTURE RESEARCH

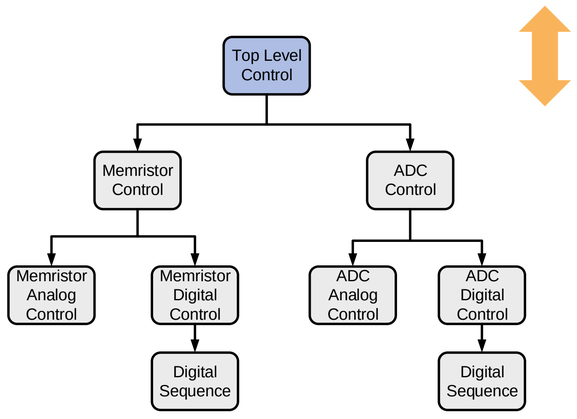
- So far, successful control of Low Resistance State (LRS) and High Resistance State (HRS) has been achieved, validating the control system's basic functionality.
- However, precise control of intermediate resistance states remains a challenge and requires further investigation to enable multi-level memory storage.
- Implementing an error correction algorithm may become essential to improve accuracy and reliability in managing these intermediate states, ensuring consistent performance across various applications.

METHODOLOGY

TOP LEVEL ARCHITECTURE

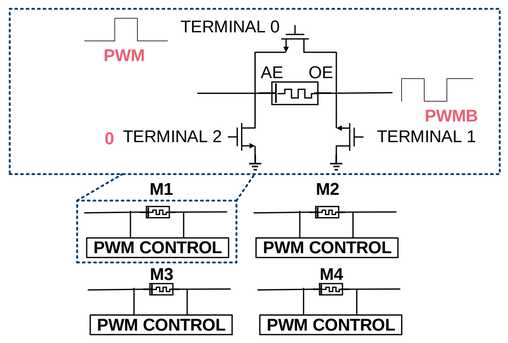


System Architecture for Controlling a 2×2 Memristor Array



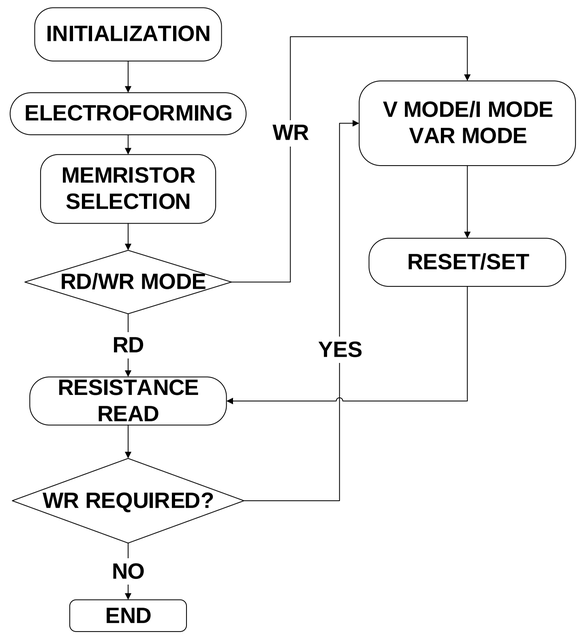
- **Top Level Control**: Directs both memristor and ADC controls.
- **Memristor Control:** Includes analog and digital control functions for setting memristor states, along with a digital sequence for operation flow.
- **ADC Control:** Manages analog and digital readout of memristor states, with a digital sequence for readout processes.

CONTROL MECHANISM



- Memristors M1, M2, M3, and M4 are arranged in a 2x2 grid and are controlled by the PWM signals generated by PWM generator.
- The PWM signals are sent to the transmission gates of the corresponding memristors to set, reset, or read each memristor.

TOP CONTROL ALGORITHM



- **Initialization:** Configure system settings and pulse parameters.
- **Electroforming:** Active the memristors.
- **Memristor Selection:** Choose the specific memristor(s) to operate on.
- **Write (WR):** Select the operation mode (Voltage, or Current) and execute the write operation.
- **Read (RD):** Measure the resistance state of the selected memristor.
- **Verification:** End the process if the memristor has reached the target state (YES). If the target state is not reached (NO), repeat the write-read sequence until successful.

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